

# Suppression of Harmonics and Common Mode Voltages in Three Level Inverter Driven Induction Motor with Dual Two Level Inverters

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**Abstract-** Power electronics applications are rapidly gaining interest among researchers to minimize the harmonic content and improve the efficiency of system. In this paper, Induction motor is driven by cascading dual two level voltage source inverter (VSI) in parallel having phase shift in their carrier waves. Phase shifted parallel dual inverter generate three level with reduced THD content and Common Mode Voltage (CMV) of 33.3% is obtained as compared to single inverter fed induction motor. This prototype is designed in MATLAB/Simulink and results are presented for speed control of induction motor.

**Index Terms-** Power electronics; total harmonic distortion; common mode voltage; voltage source inverter; induction motor.

## 1. INTRODUCTION

About 70% of the industrial load consists of squirrel cage induction motor. Speed control of induction motor was tricky prior to advancement in power electronics devices. However, with advancement in power electronics devices and hence converters, induction motor drives are gaining importance (Tolbert et al., 1999; 2000). Variable magnitude and frequency is easily achievable with the help of pulse width modulated inverters for speed control of induction motor (Srinivas and Ramachandra Sekhar, 2013; Buja and Kazmierkowski, 2004).

Mostly, control of the Inverters is done with switching of power semi conductor devices. Inverters employing semiconductor devices offer numerous advantages of long life span, compact size, flexible operation because of digital control, fast dynamic response, fast switching devices for high efficiency.

However, these semi conductor switching devices generate voltage and current harmonics into the supply system. (Prabaharan and Palanisamy, 2017) These harmonics are unavoidable that affects the load connected with these converters. They can cause distortion of the output voltage, increase THD and Electromagnetic Interference (EMI) related issues (Du et al., 2008; Santhakumar et al., 2017). It is essential to reduce the harmonic level to a tolerable magnitude on input as well as output side. For AC applications especially for motor drives, Common Mode Voltage (CMV) (Hava and Un, 2009) and Total Harmonic Distortion (THD) measure is essential. Total Harmonic distortion is

the ratio of root of sum of all square of all harmonic components to RMS value of the fundamental component.

$$THD = \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + \dots + \infty}}{V_1}; \text{ where } V_1$$

is fundamental component and  $V_2, V_3, V_4, \dots$  are harmonic components of 2<sup>nd</sup>, 3<sup>rd</sup>, 4<sup>th</sup>, ..... harmonics. Common Mode Voltage (CMV) is voltage between neutral point of load and dc midpoint/system ground. It is also defined as an average voltage passing through neutral.

Multilevel Inverters with high switching frequency reduce the THD (Du et al., 2008; Kouro et al., 2010) improving the quality of output (Eltamaly, 2008). However, multilevel Inverters have their limitations due to capacitor balancing, voltage unbalance, cost and complexity in system (Prabaharan and Palanisamy, 2017; Prakash et al., 2016). Moreover, multilevel inverters cannot meet demand of mega volt-ampere ratings (Tolbert, Peng and Habetler, 1999). In addition, practical switches, incur energy loss while opening and closing of switch hence restraining the switching frequency (Baiju et al., 2004). This captivates the authors to explore Inverters for better overall efficiency of the system with minimum distortion in output waveform. The current and voltage waveforms govern the quality of converter. Control strategy directly governs the THD and can be selected indigenously to minimize or reduce these problems.

Pulse width modulation (PWM) (Holtz, 1992) is the basis for control in power electronics. Common modulation strategies are:

1. Sinusoidal Pulse Width Modulation (SPWM)
2. Selective Harmonic Elimination Pulse Width Modulation (SHEPWM)
3. Space Vector Pulse Width Modulation (SVPWM)

## 2. PARALLEL PHASE SHIFTED DUAL INVERTERS

The schematic of dual Inverter feeding induction motor is illustrated in Figure 1. This prototype consists of dual two level Inverters connected in parallel. Single unit of three-phase voltage source Inverter has limited power handle capacity, which can overcome by employing multiple modules of Inverter. In this paper, two units of Inverters are connected in parallel with phase shift in carrier

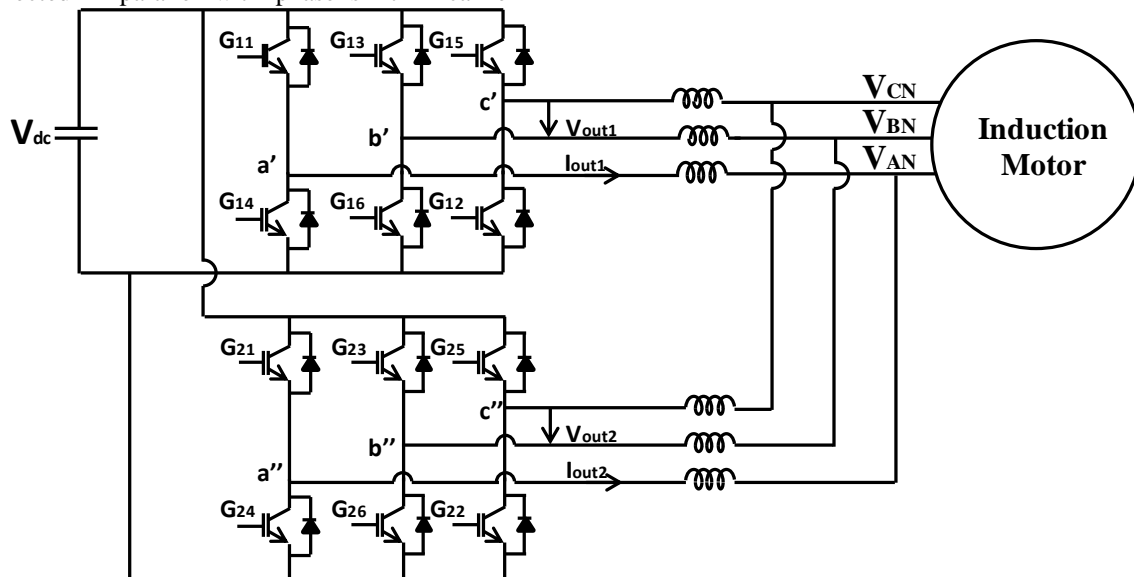


Fig. 1. Dual two level voltage source inverters connected in parallel feeding induction motor

Switching in each leg should not occur simultaneously in order to avoid short circuit across DC link. Switching in three legs is displaced by  $120^\circ$ . The desired output voltage with low THD is obtained by performing multiple switching with constant DC voltage. Switching states and number of switches connected in a prototype depends upon load requirements. For dual Inverter,  $2 \times 6$  switch matrix needs to be controlled in effective way to reduce switching losses. Freedom of disparate switching sequence enables to obtain desired output waveform. The output with SPWM topology is obtained with phase shift for Inverter 2 and employing similar switching of Inverter 1 omitting the computations required.

Among these modulation techniques, SPWM (Holtz, 1994) is used in this paper because of simple and fast computation as compared to SHEPWM and SVPWM. This paper is organized as follow. Section 2 discusses parallel phase shift topology employed to Dual inverters. Section 3 analyzes results obtained for single as well as dual inverter fed inverter. Section 4 concludes the merits of phase shifted dual inverter over single inverter.

waves. Each Inverter is fed from same common uncontrolled rectifier. Inverter is modelled with IGBT's due to its inherent advantage of high voltage, high current for high frequency applications. In three phase Inverter (shown in Figure 1),  $2 \times 3$  switch matrix with full bridge is required for two level voltage generation (Varjani et al., 1998).

For SPWM, a high frequency ( $f_c$ ), triangular carrier wave is compared with sinusoidal modulating wave of desired frequency ( $f_m$ ). The intersection of two waves determines the switching instants and commutation of modulated pulse. Inverter 1 and Inverter 2 are connected in parallel via inductors in order to eliminate circulating currents. Inverter 1 compares modulating reference signal with triangular carrier wave. Inverter 2 compares same three phase modulating signal with phase shifted carrier wave for all the three phases. Phase shift should be indigenously selected (Mwinyiwiwa, Wolanski and Ooi, 1998) in order to get best results.

Parallel phase shifted dual inverters gives exceptional results over single inverter fed induction motor and these features are listed as:

- Linear amplification is obtained with VSI (Mwinyiwiwa, Wolanski and Ooi, 1996)
- Virtual rise in frequency is observed, thereby reduces switching losses (Mwinyiwiwa, Wolanski and Ooi, 1999)
- THD content is reduced
- Harmonics are shifted on to higher side, easy to filter and are less hazardous

### 3. RESULTS AND DISCUSSION

In this paper, SPWM parallel phase shifted dual inverter feeding induction motor is simulated in Simulink shown in figure 2. . Induction motor of 3.7 kW, 415V, 7.4A, 50Hz with rated speed of 1500 r.p.m is simulated to validate the parallel phase shift dual inverter topology. Simulation results are

- CMV is reduced significantly
- Ripple content in current is reduced
- Redundancy of parallel inverters for speed control of induction motor
- High mega volt-ampere ratings can be obtained with parallel dual inverters (Singh *et al.*, 2005)

obtained with MATLAB 2013a with Tustin solver and sample time of 50µsec. Switching frequency of 3.63 kHz for carrier wave 1 and carrier wave 2 with modulation index of 0.8 is employed in this paper. While simulating VSI Inverter, CMV and THD are plotted and analyzed for single inverter as well as parallel dual inverter fed induction motor.

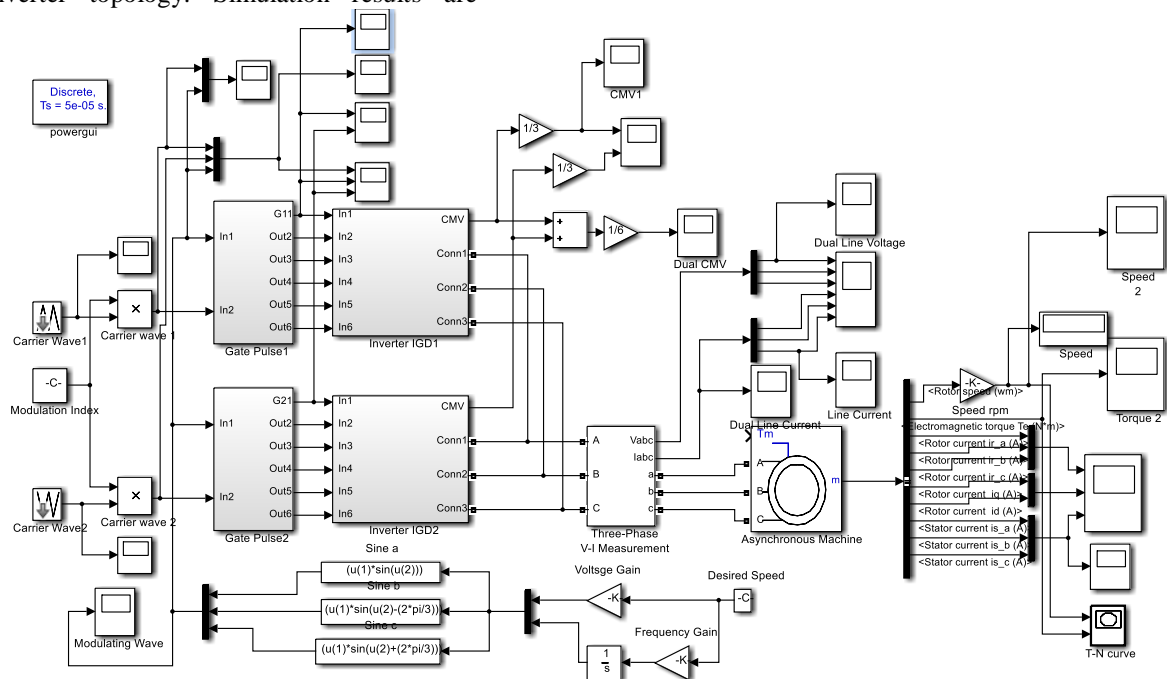
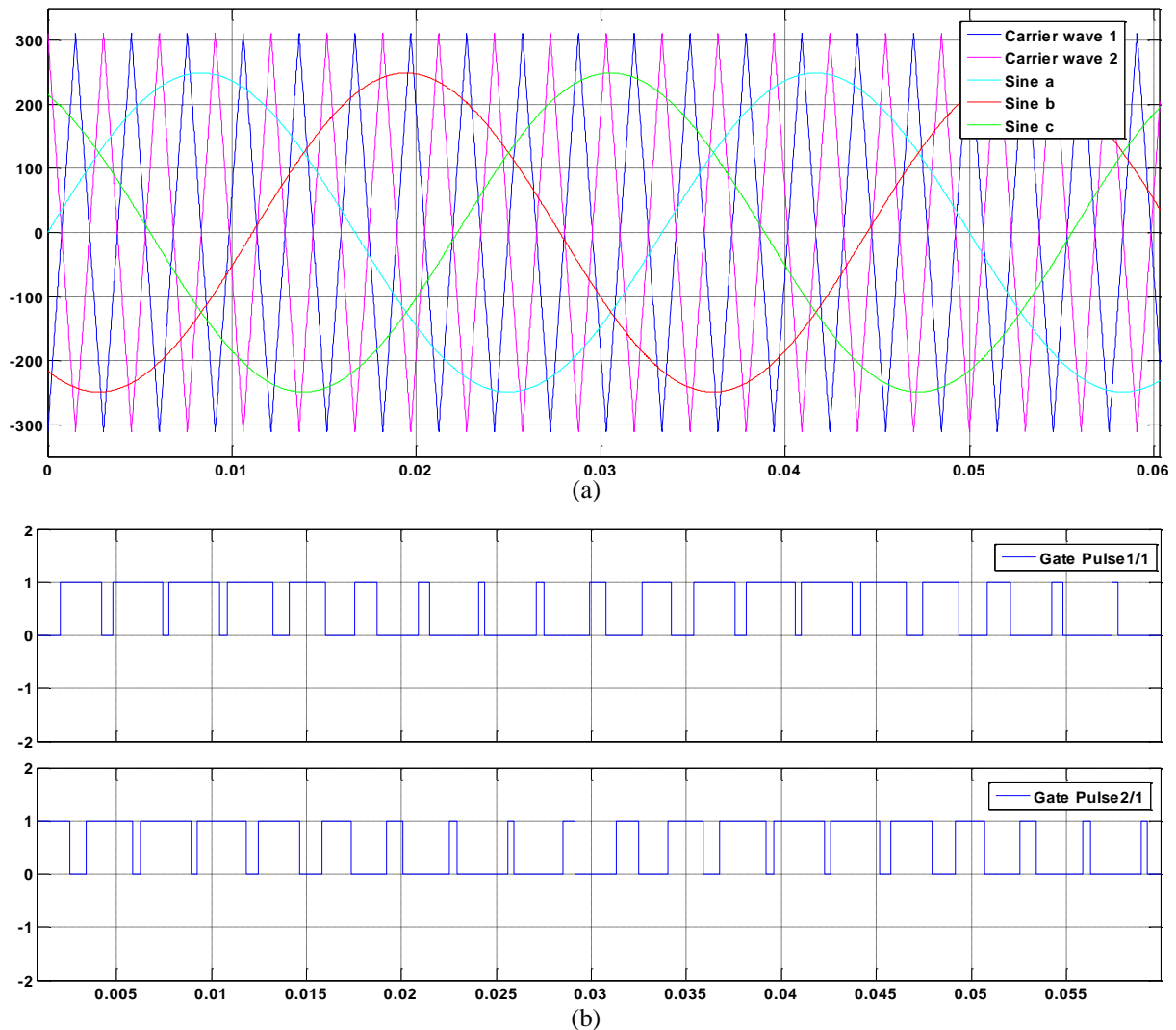


Fig. 2 Phase shifted parallel dual inverter modelled in Matlab/Simulink

While employing phase shifted parallel inverters, same modulating signal is compared with phase

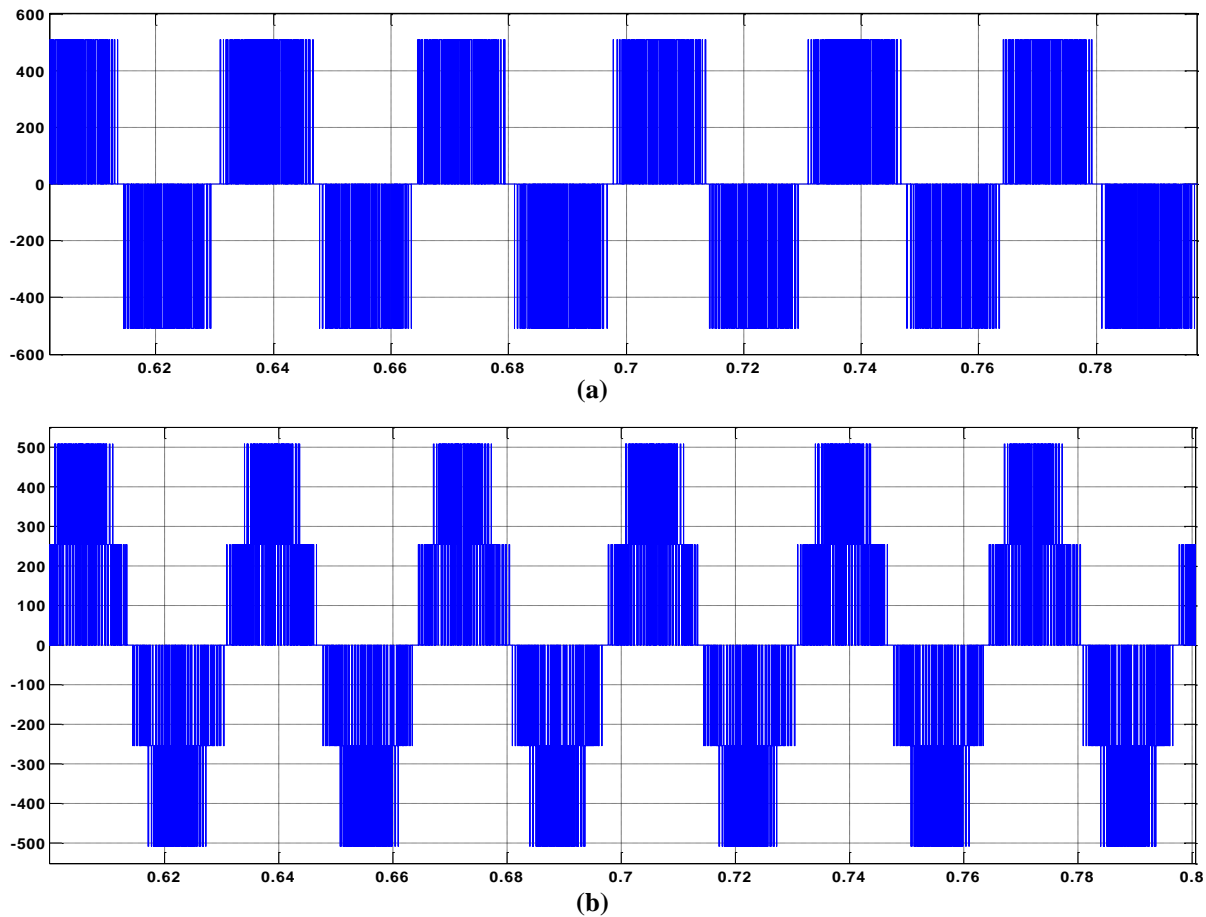
shifted carrier waves as shown in fig 3. Phase shifted gate pulses are obtained.



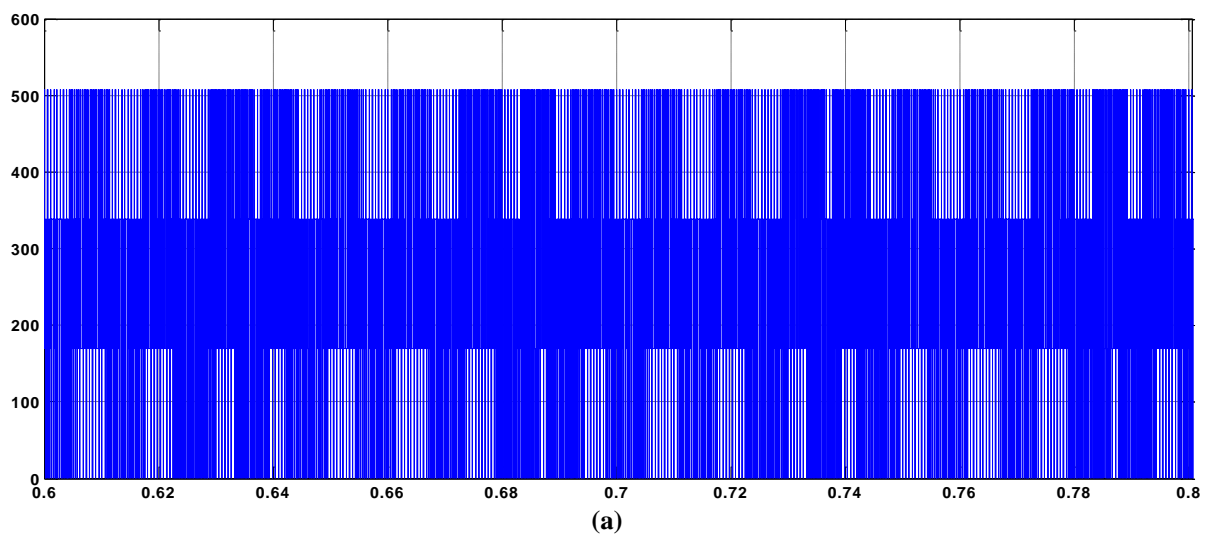
**Fig 3:** (a) Simulation results obtained for three phase modulating waveform and phase shifted carrier wave (b) Corresponding Gate Pulse obtained for inverter 1 and inverter 2

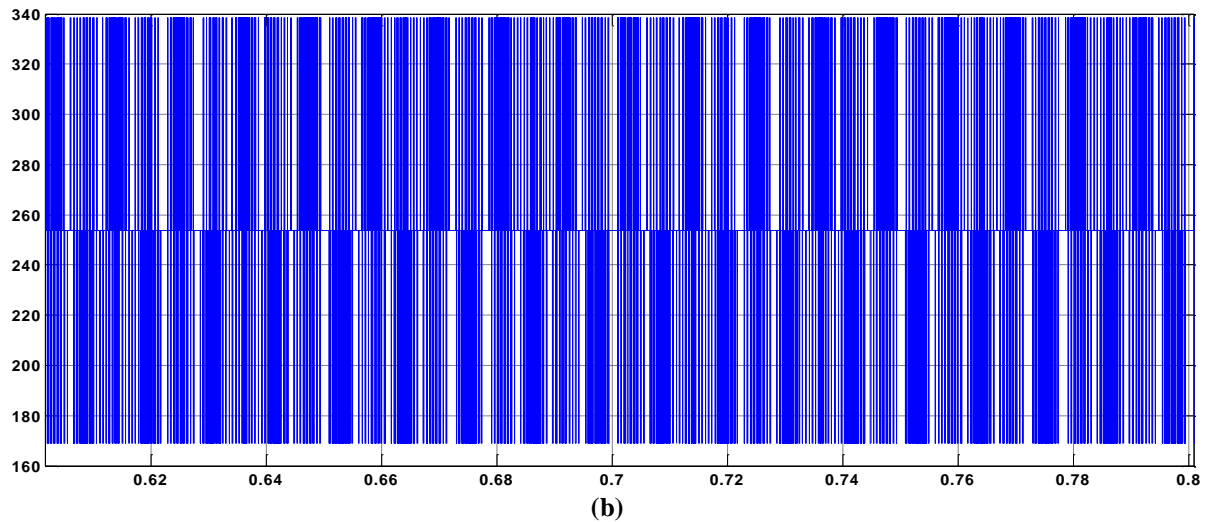
Single inverter with total of six switches generate two level line voltage as shown in figure 4. However, parallel phase shifted dual inverter generate three level line voltage at ac terminal. Common mode voltage is also obtained for single inverter as well as dual inverter shown in figure 5. It is clearly observed that CMV for single inverter

is levelled from 0 to  $V_{dc}$  whereas CMV for dual inverter is only between  $\frac{1}{3}V_{dc}$  to  $\frac{2}{3}V_{dc}$ . A significant reduction of 66.6 % of CMV is obtained with phase shifted parallel dual inverter feeding induction motor.



**Fig 4:** (a) Simulation results obtained with SPWM for (a) line voltage from two level inverter (b) line voltage of three level from parallel dual inverter

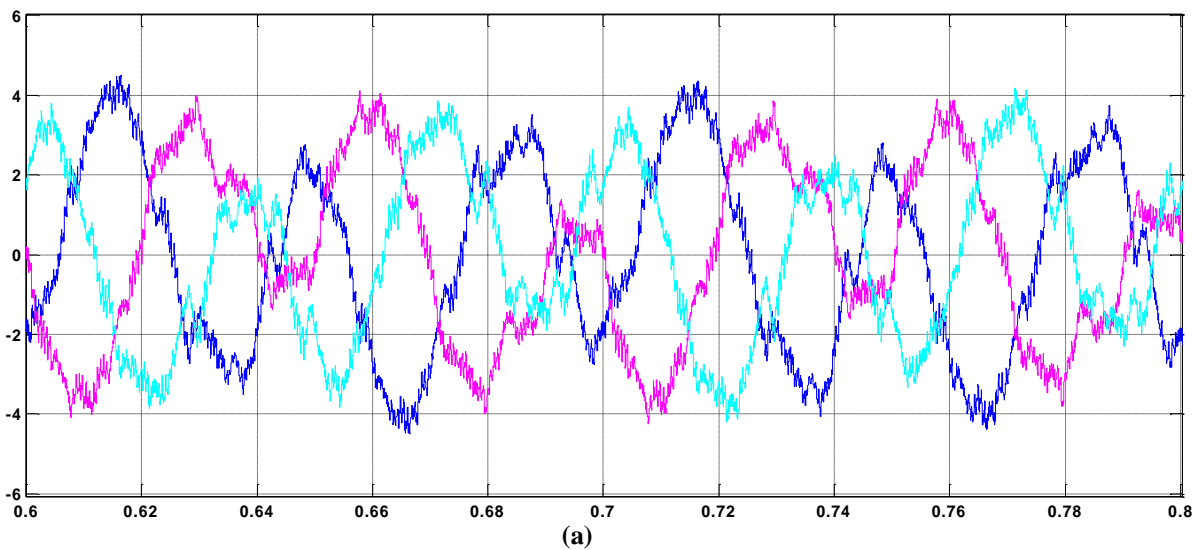


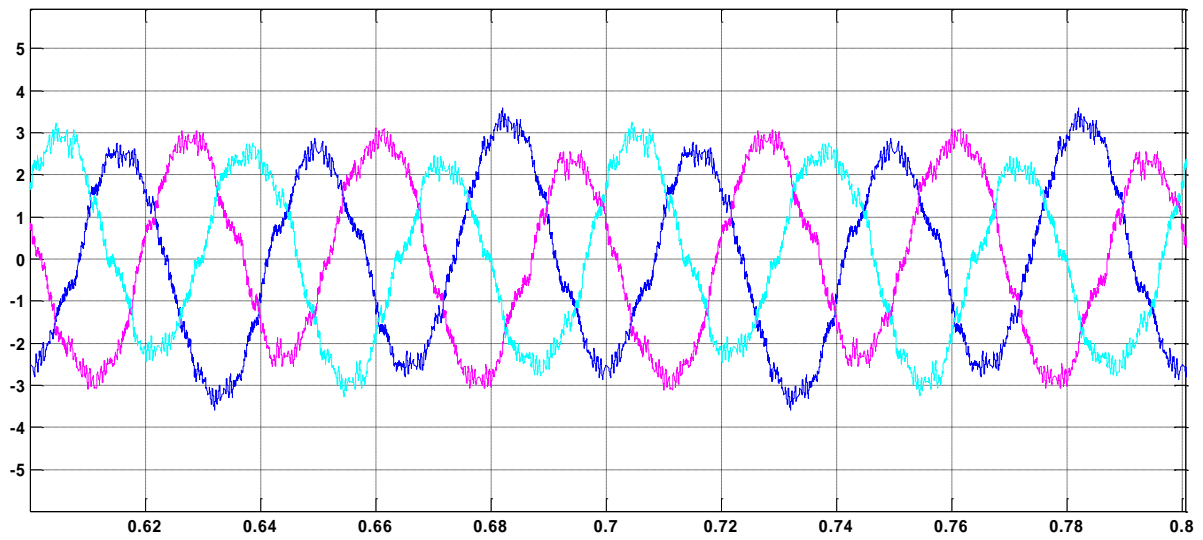


**Fig 5:** Common mode voltage with SPWM obtained with Simulink for (a) two level inverter (b) parallel dual inverter

Ripple content in line current at ac terminal of inverter for single inverter as well as dual inverter is shown in figure 6. Dual inverter produces more

sinusoidal waveform with lesser ripples as compared to single inverter.



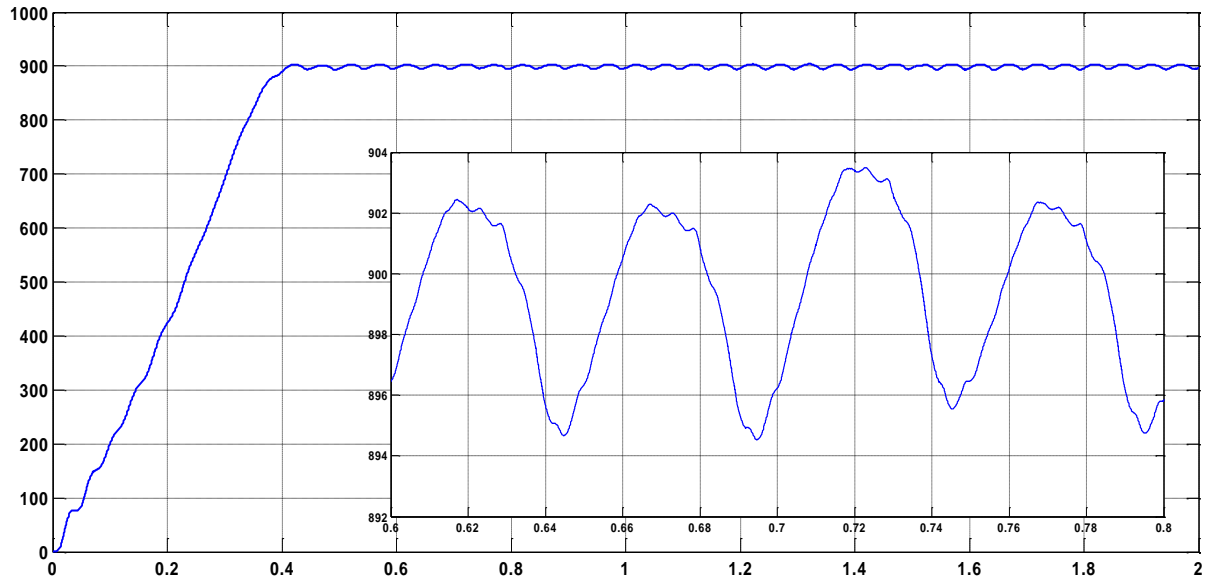


(b)

**Fig 6:** Current at ac terminal with SPWM for  $m_a=0.8$  for (a) Single inverter (b) dual inverter

Speed control of induction motor with variable voltage and frequency is obtained with single as well dual inverter achieved is shown in figure 7. Induction motor is operated at 900 r.p.m. Single inverter fed induction motor shows speed fluctuations between 894 to 904

r.p.m. Dual inverter gives more stable speed with variation from 898 to 900 r.p.m. only. This stable speed gives stable torque and hence improves the performance of induction motor.



(a)

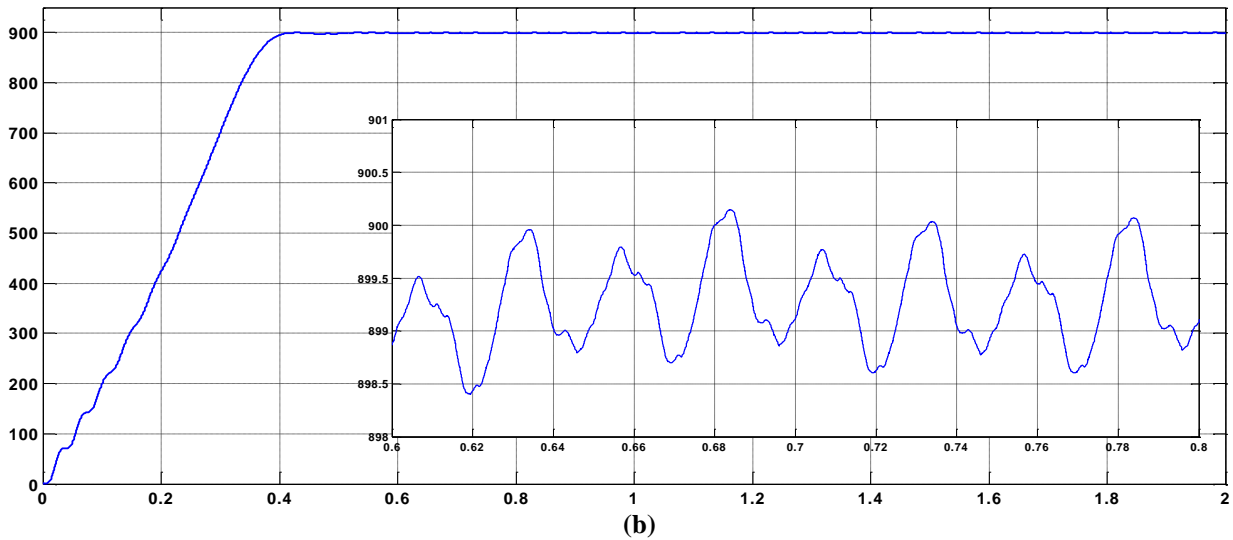


Fig 7: Speed control of induction motor Obtained at 900 rpm with SPWM for (a) single inverter (b) dual inverter

The proposed phase shift topology is verified over wide speed range of induction motor at different modulation indices summarized in figure 8.

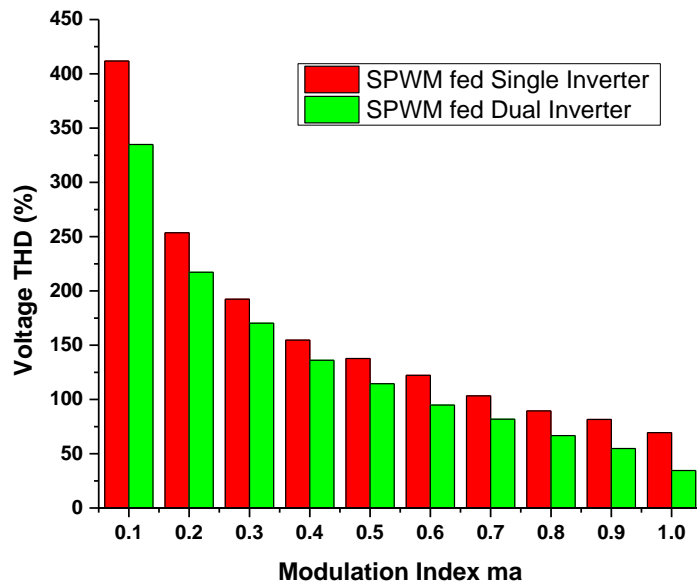


Fig 8: Comparison of voltage THD for modulation index range from 0.1 to 1

#### 4. CONCLUSION

In this paper, parallel phase shifted dual inverter for speed control of induction motor has been simulated in Matlab/Simulink. Simulated results are obtained showing significant improve in performance of induction motor while driven from dual inverter. Phase shift in inverters generate three

level output voltage while cascading two level inverters. Better voltage profile with reduced THD content is obtained at ac terminal of dual inverter. This gives more stable speed and hence stable torque operation of induction motor. CMV is reduced significantly by 66.6% with parallel phase shifted dual inverters. Owing to reduction in THD and CMV, filter requirement is minimized reducing



the cost of overall system. Parallel phase shifted inverters can boost power handling capability with

reduced switching losses.

### **Acknowledgements**

Authors would like to thank IKGPTU, Kapurthala for providing the access to journals and papers required for research work.

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